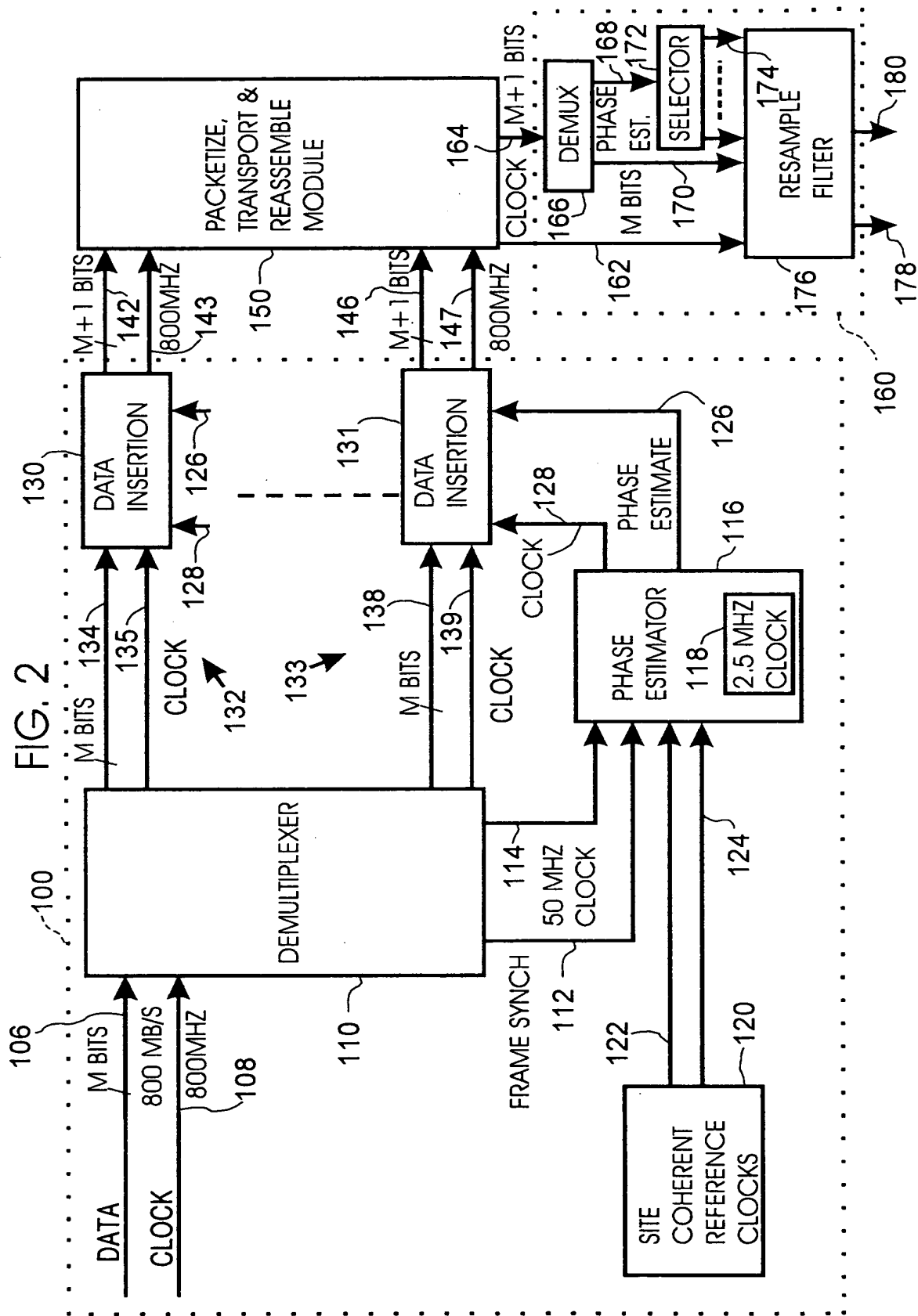


The diagram illustrates a digital signal processing system, likely for a digital subscriber line (DSL) receiver, designed to handle phase differences between a data clock and a reference clock. The system is divided into several functional blocks and signal paths:

- Data Path (Left Side):** A dashed box labeled **10** contains a **DATA SOURCE** (14) and a **DATA CLOCK** (16). The data source provides **M BITS** (18) to a **MUX & BUFFER** (30). The data clock (16) is also connected to the MUX & BUFFER (30) and a **PHASE DIFFERENCE ESTIMATOR** (22).
- Reference Clock Path (Right Side):** A **REFERENCE CLOCK(S)** (24) provides a **REFERENCE** (26) to the **PHASE DIFFERENCE ESTIMATOR** (22).
- Phase Difference Estimation:** The **PHASE DIFFERENCE ESTIMATOR** (22) receives inputs from the data clock (16) and the reference clock (26) to calculate **PHASE DIFFERENCES** (28).
- Asynchronous Transport:** The **PHASE DIFFERENCES** (28) are sent to the **MUX & BUFFER** (30) via an **ASYNCHRONOUS TRANSPORT** (32). This path is separated from the rest of the system by a dotted line labeled **40**.
- Processing Path (Right Side):** The output from the MUX & BUFFER (30) goes to a **BUFFER & DEMUX** (46). A **CLOCK** (42) is provided to the buffer/demux (46) and a **RESAMPLE (INTERPOLATE) FILTER (FIR)** (50). The buffer/demux (46) outputs **M+L BITS** (51) to the resample filter (50). The resample filter (50) is connected to a **COEFFICIENT ROM** (56) via a dashed line (52). The coefficient ROM (56) is connected to an **ADDRESS INTERFACE** (60) via a line (58). The address interface (60) is connected to the resample filter (50) via a line (54).



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